**ANNA UNIVERSITY :: CHENNAI – 600 025**

**MODEL QUESTION PAPER**

VI - SEMESTER

B.E. ELECTRICAL AND ELECTRONICS ENGINEERING

**EE350 - COMPUTER ARCHITECTURE**

**Time: 3hrs** **Max Marks: 100**

**Answer all Questions**

**PART – A (10 x 2 = 20 Marks)**

1. What is MAR and MBR? What will be the content of MAR and MBR for read and write operation?

2. Define stack. Following operations were performed on stack, which contains an integer item 10.
   Push 20, Push 30, Pop, Push 40, Pop, Pop.
   What will be the top element of stack after above all operations were completed?

3. Explain with an example, the 2's compliment subtraction.

4. Define Bit-slice processing. What is a bit slice?

5. RISC processors typically have instructions of equal size. What is advantage of such choice?

6. Define micro instruction and micro program.

7. What is the need for memory hierarchy?

8. Define hit ratio. Give the relation between hit ratio and access efficiency.

9. What is an interrupt? Mention its need.

10. Draw block diagram of DMA controller.

**PART – B (5 x 16 = 80 Marks)**

11. (i) Discuss about the various instruction formats. (8)

    (ii) Explain stack organization. (8)

12.a) Draw and explain the flow chart of floating point arithmetic operation for addition and subtraction. (16)

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**OR**

b) Explain Booth algorithm for multiplying two binary numbers. (16)

13.a) Explain about micro programmed control unit with a neat diagram. (16)

**OR**

b) Design a computer with 512 bytes of RAM 1024 bytes of ROM. The memory is available in 128 bytes RAM chips and 512 bytes of ROM chips. Select appropriate size address and data buses. If needed decoders can be used. Draw the connection and show the address mapping. (16)

14.a)i) Define virtual memory. What is the necessity for using the concept of virtual memory? (16)

ii) Explain with a neat diagram how address mapping is done in paging system. (16)

**OR**

b) Define Cache memory. Explain anyone mapping procedure. (16)

15.a) Explain programmed IO system and IO processor. (16)

**OR**

b) (i) Discuss an IO processor and its organization. (12)

(ii) Explain how priority in interrupts are handled. (4)

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